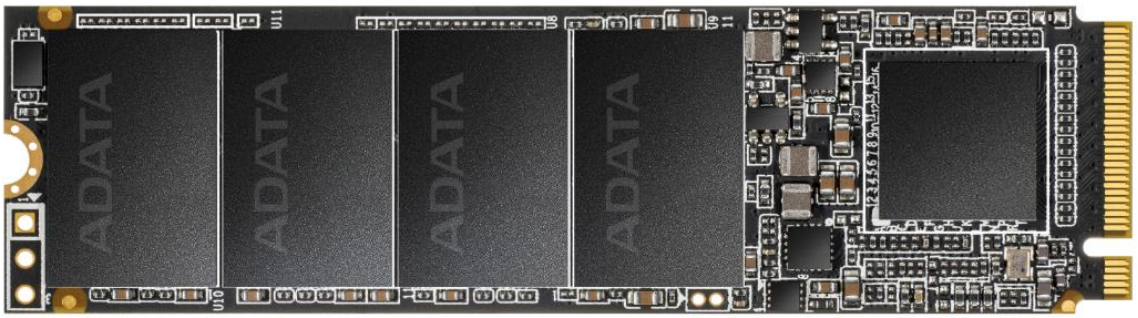
M.2 2280 PCIe SSD



(Photo for reference only.)

Version 1.3

Oct. 25, 2021

SM2P32A8

256GB, 512GB, 1TB

Revision History

Revision	Date	Description	Editor
1.0	Apr. 23, 2021	Initial release	Marx Yang
1.1	May. 11, 2021	Update for requirements	Marx Yang
1.2	Jun. 8, 2021	Update CMD and SMART tables; Update FW version; Add Data Retention, Power Up, and PCIe Power Management Register Tables	Marx Yang
1.3	Oct. 25, 2021	Update 3.4 Power consumnption, 3.8 FW version, 6.0 SSD Label	Cindy Lee

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Key Features

- **Capacity:**
  - 256GB, 512GB, 1TB
- **NAND Flash:** 3D NAND
- **Form Factor:** M.2 2280 PCIe
- **Host Interface:**
  - PCIe Gen 3 (8Gb/s) x 4 Lane
  - Compliant with NVMe 1.3 register interface and command set
  - Compliant with PCIe Express 3.1
- **Flash Management:**
  - LDPC ECC Engine
  - Wear leveling
  - Bad block Management
  - Garbage collection
  - TRIM Command
  - SLC Cache Technology
- **Security:**
  - AES 256 supported
- **Data Integrity:**
  - Thermal throttling
  - S.M.A.R.T. monitor
- **Performance:**
  - Sequential Read: Up to 3400 MB/s
  - Sequential Write: Up to 2100 MB/s
  - Random 4K Read: Up to 100K IOPS
  - Random 4K Write: Up to 190K IOPS
- **Power Consumption:**
  - L0 : 0.55w
  - L1 : 0.04w
  - L1.2 : 0.0013w
  - SR/SW : 1.61w/2.63w
  - RR/RW: 1.59w/1.77w
- **Temperature:**
  - Standard: 0°C ~ 70°C
  - Non-operation: -40°C ~ 85°C
- **Reliability:**
  - Shock: 1500G/0.5ms
  - Vibration 20G Peak, 10~2000Hz
  - MTBF: 2,000,000 hours
  - Uncorrectable Bit Error Rate(UBER): 10^{-15}
- **Endurance:**
  - TBW: Up to 960TB

1.0 General Description

To replace the SATA SSD, look no further than the SM2P32A8 PCIe Gen3x4 M.2 2280 SSD. Supporting NVMe 1.3, equipped with 3D NAND Flash, and coming with up to 1TB capacity, the SM2P32A8 is a great upgrade choice.

Featuring HMB (Host Memory Buffer) and SLC Caching, the SM2P32A8 accelerates read/write speeds up to 3400/2100MB/s and delivers random performance of up to 100K/190K IOPS. Whether booting, gaming or transferring large files, the SM2P32A8 accomplish them quickly and effectively.

The SM2P32A8 utilizes LDPC (Low-Density Parity-Check) error correcting code technology to detect and fix a wider range of data errors for more reliable data transfers and a longer product lifespan. Also, it is suitable for desktop and notebook PCs. As there’s no need for cumbersome installation, you can immediately experience the high speed and smoothness of a PCIe SSD.

2.0 Mechanical Specifications

All product specifications not covered in this document (electrical performance, appearance, etc.) are in accordance with ADATA's defined norms and standards.

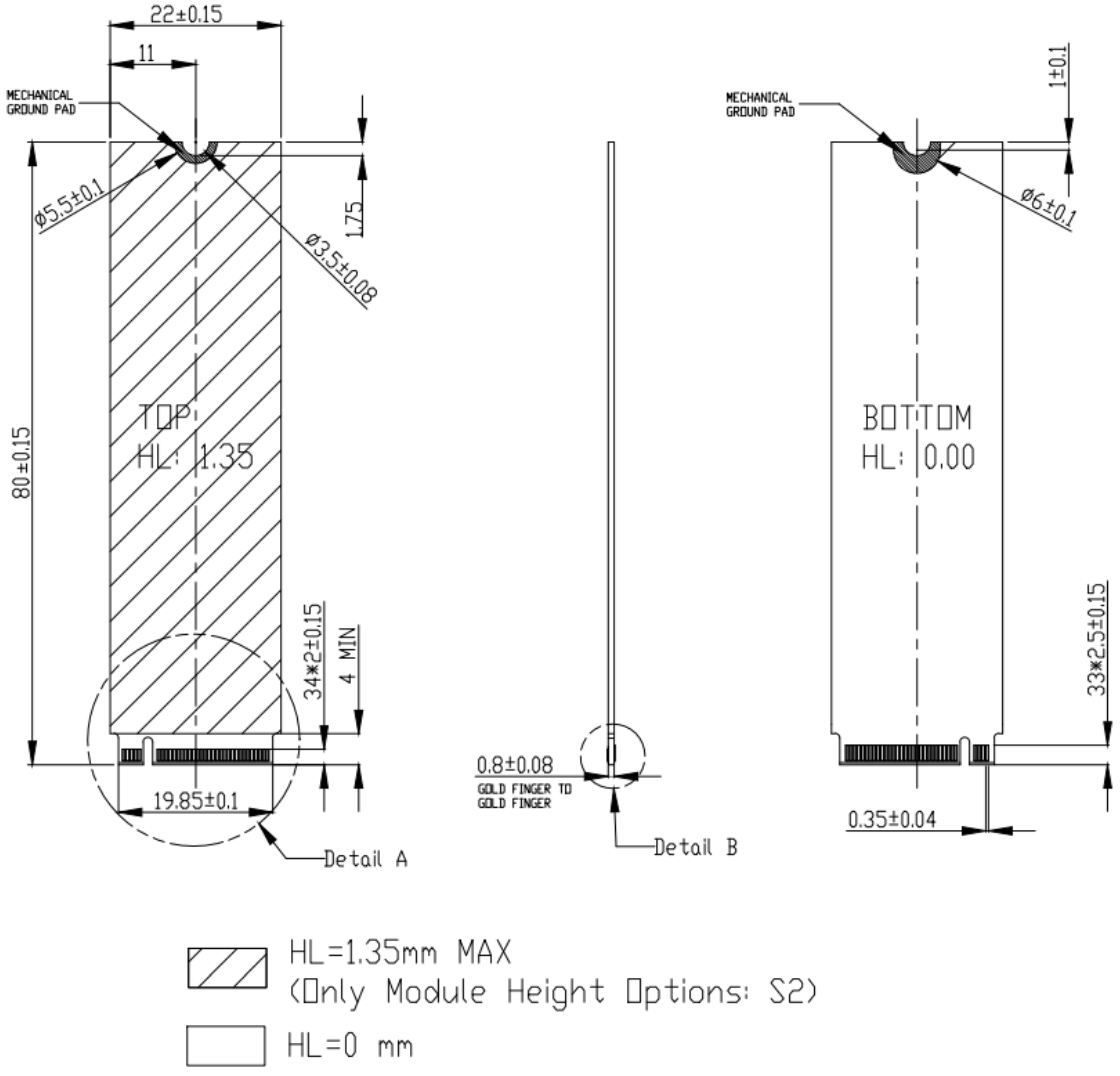
2.1 Physical Dimensions and Weights

Table 2-1 Dimensions and Weights

Capacity(GB)	Length(mm)	Width(mm)	Height(mm)	Weight(gram)
256GB	80.00±0.15	22.00±0.15	Max 2.15	Max 7
512GB	80.00±0.15	22.00±0.15	Max 2.15	Max 7
1TB	80.00±0.15	22.00±0.15	Max 2.15	Max 7

2.2 Product Dimensions

Figure 2-1 Product Dimensions



3.0 Product Specifications

3.1 Interface and Configurations

- Compliant with PCI Express M.2 Specification Revision 1.1.
- Compliant with NVMe 1.3 register interface and command set.
- Compliant with PCIe Express 3.1

3.2 Capacity

Table 3-1 User Addressable Sectors

Model	SM2P32A8		
Unformatted Capacity	256GB	512GB	1TB
Total User Addressable Sectors (LBA Mode)	500,118,192	1,000,215,216	2,000,409,264

Total useable capacity may be less (duo to formatting, flash management, and other functions).
1GB=1,000,000,000 bytes; 1sector = 512bytes.

3.3 Performance

3.3.1 ATTO Performance

Table 3-2 Read/Write Performance (ATTO)

	256GB	512GB	1TB	Unit
Sequential Read	3200	3300	3300	MB/s
Sequential Write	1200	1900	2000	MB/s

-Seq. Read & Write speed test by ATTO
-The system conditions and test environment may affect test result

3.3.2 CDM Performance

Table 3-3 Read/Write Performance (CDM)

	256GB	512GB	1TB	Unit
Sequential Q32 Read	3200	3400	3400	MB/s
Sequential Q32 Write	1200	1900	2100	MB/s
4K-QD64 Read	380	370	390	MB/s
4K-QD64 Write	540	530	540	MB/s

-Seq. Read & Write speed test by Crystal Disk Mark 6.0.2

3.3.3 IOPS Performance

Table 3-4 Read/Write IOPS Performance

	256GB	512GB	1TB	Unit
4K Random Read	90K	100K	100K	IOPS
4K Random Write	140K	160K	190K	IOPS

-Seq. Read & Write speed test by IOmeter 2010 with “00” pattern (Queue depth of 64; Measurements are performed on 10% capacity of LBA range. Write cache enable)
-IOPS Queues/Threads: Q64T8
-Different system conditions and test environments may affect test results

3.3.4 AS-SSD Performance

Table 3-5 Read/Write Performance (AS-SSD)

	256GB	512GB	1TB	Unit
Sequential Read	2700	2800	2700	MB/s
Sequential Write	1100	1700	1800	MB/s
4K-64 Thrd Read	380	390	390	MB/s
4K-64 Thrd Write	890	960	950	MB/s

-Seq. Read & Write speed test by AS-SSD with Random pattern

3.4 Electrical Specifications

3.4.1 Operating Voltage

Table 3-6 Operating Voltage

Operating Voltage	
Input Power	DC 3.3V ± 5%
Maximum Allowable Ripple	100mV p-p

3.4.2 Power Consumption

Table 3-7 Power Consumption (Typical)

	256GB	512GB	1TB	Unit
L0	0.55	0.54	0.55	**W**
L1	0.04	0.04	0.04	**W**
L1.2	0.0013	0.0013	0.0013	**W**
Sequential Read	1.60	1.56	1.61	**W**
Sequential Write	2.12	2.43	2.63	**W**
Random Read	1.60	1.54	1.59	**W**
Random Write	1.73	1.74	1.77	**W**

3.5 Environmental Conditions

Table 3-8 Temperature and Humidity

Feature	Operating	Non-Operating
Standard Temperature	0°C to 70°C	-40°C to 85°C
Humidity	5%~95% RH, non-condensing	

3.6 Reliability

Table 3-9 Shock and Vibration

Parameter	Conditions	Reference Standards
Shock	1500G, 3 axes, duration 0.5ms, Half Sine Wave	JESD22-B110
Vibration	20G , 3 axes , Peak, 20~2000Hz	JESD22-B103

Table 3-10 MTBF

Parameter	Conditions	Hours
MTBF	MIL-HDBK-217	2,000,000

Table 3-11 Uncorrectable Bit Error Rate

Parameter	Value
Uncorrectable Bit Error Rate (UBER)	1 sector in 10^{-15} bits read, Max

Table 3-12 ESD Test

Basic Standard	EN 61000-4-2/ IEC 61000-4-2
Test Level	Contact +/- 4KV Air +/- 2KV, +/- 4KV, +/- 8KV
Criteria	Class B

Table 3-13 EMI Test

Parameter	Conditions	Result
EMI	CISPR22 CISPR32	Class B

Table 3-14 Data Retention

Parameter	Value
Data Retention	30˚C / 1 year

3.7 Endurance

SSD endurance can be predicted based on the operating workload. The table below shows the drive lifetime for each SSD capacity based JESD219 client workload.

Table 3-15 Terabytes Written

Capacity	256GB	512GB	1TB	Unit
TBW	240	480	960	TB

3.8 FW Version

Table 3-16 FW Version

	256GB	512GB	1TB
FW Version	VC0S0304	VC0S0304	VC0S0304

3.9 Key Component List

Table 3-17 Key Component List.

	256GB	512GB	1TB
CTL	Realtek RTS5766DL	Realtek RTS5766DL	Realtek RTS5766DL
DRAM	No DRAM	No DRAM	No DRAM
Flash	Micron B47R 512Gb	Micron B47R 512Gb	Micron B47R 512Gb

3.10 Thermal Specifications

Table 3-18 Thermal Specifications

Condition	SMART Drive Temperature	CTL T-Junction Temperature
Light throttling	80 ˚C	100 ˚C
Heavy throttling	90 ˚C	110 ˚C
Trickle IO	95 ˚C	115 ˚C

3.11 Power Up Specifications

Table 3-19 Power Up Specifications

Parameter	Value
POR (Power-On-Ready)	1.89 second
SPOR (Sudden Power-On-Ready)	3.5 second

- Complete the first I/O command (PERST→ First I/O)

3.12 PCIe Power Management Register

Table 3-20 PCIe Power Management Register

Parameter	Value
Power Management Register	ASPM L1 supported, L1 PM Substates supported, ASPM L1.1 supported, ASPM L1.2 supported, PCI-PM L1.1 supported, PCI-PM L1.2 supported

4.0 Support Command Sets

4.1 Identify Device Command

ADATA SSD follows NVMe 1.3 Specification and responds to identify command with a pre-defined string of information listed in Identify Controller Data structure.

Table 4-1 Identify Controller Data Structure Table

Bytes	O/M	Default Value	Description
Controller Capabilities and Features			
01:00	M	0x10ec	PCI Vendor ID (VID)
03:02	M	0x10ec	PCI Subsystem Vendor ID (SSVID)
23:04	M	“xxxxxxxxxxxx”	Serial Number, #:Variables
63:24	M	“SM2P32A8-XXXGC”	Model Number (MN)
71:64	M	VC0S0304	Firmware Revision, #:Variables
72	M	0x00	Recommended Arbitration Burst (RAB)
75:73	M	0x00e04c	IEEE OUI Identifier (IEEE)
76	O	0x00	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)
77	M	0x05	Maximum Data Transfer Size (MDTS)
79:78	M	0x0001	Controller ID (CNTLID)
83:80	M	0x00010400	Version (VER)
87:84	M	0x000f4240	RTD3 Resume Latency (RTD3R)
91:88	M	0x001e8480	RTD3 Entry Latency (RTD3E)
95:92	M	0x00000300	Optional Asynchronous Events Supported (OAES)
99:96	M	0x00000002	Controller Attributes (CTRATT)
111:100		Reserved	
127:112		0x00000000	FRU Globally Unique Identifier (FGUID)
239:128		Reserved	
255:240		Refer to the NVMe Management Interface Specification for definition.	
Admin Command Set Attributes & Optional Controller Capabilities			
257:256	M	0x0017	Optional Admin Command Support (OACS)
258	M	0x00	Abort Command Limit (ACL)
259	M	0x03	Asynchronous Event Request Limit (AERL)
260	M	0x02	Firmware Updates (FRMW)
261	M	0x03	Log Page Attributes (LPA)
262	M	0x07	Error Log Page Entries (ELPE)
263	M	0x04	Number of Power States Support (NPSS)
264	M	0x01	Admin Vendor Specific Command Configuration (AVSCC)

265	O	0x01	Autonomous Power State Transition Attributes (APSTA)
267:266	M	0x0184	Warning Composite Temperature Threshold (WCTEMP)
269:268	M	0x0189	Critical Composite Temperature Threshold (CCTEMP)
271:270	O	0x0014	Maximum Time for Firmware Activation (MTFA)
275:272	O	0x00004000	Host Memory Buffer Preferred Size (HMPRE)
279:276	O	0x00002000	Host Memory Buffer Minimum Size (HMMIN)
295:280	O	0x00000000	Total NVM Capacity (TNVMCAP)
311:296	O	0x00000000	Unallocated NVM Capacity (UNVMCAP)
315:312	O	0x00000000	Replay Protected Memory Block Support (RPMBS)
317:316	Reserved		
318	O	0x01	Device Self-test Options (DSTO)
319	M	0x01	Firmware Update Granularity (FWUG)
321:320	M	0x04b0	Keep Alive Support (KAS)
323:322	O	0x0001	Host Controlled Thermal Management Attributes (HCTMA)
325:324	O	0x0111	Minimum Thermal Management Temperature (MNTMT)
327:326	O	0x0189	Maximum Thermal Management Temperature (MXTMT)
331:328	O	0x00000000	Sanitize Capabilities (SANICAP)
511:322	Reserved		
NVM Command Set Attributes			
512	M	0x66	Submission Queue Entry Size (SQES)
513	M	0x44	Completion Queue Entry Size (CQES)
515:514	M	0x0004	Maximum Outstanding Commands (MAXCMD)
519:516	M	0x00000001	Number of Namespaces (NN)
521:520	M	0x001c	Optional NVM Command Support (ONCS)
523:522	M	0x0000	Fused Operation Support (FUSES)
524	M	0x00	Format NVM Attributes (FNA)
525	M	0x05	Volatile Write Cache (VWC)
527:526	M	0x0000	Atomic Write Unit Normal (AWUN)
529:528	M	0x0000	Atomic Write Unit Power Fail (AWUPF)

530	M	0x01	NVM Vendor Specific Command Configuration (NVSCC)
531	M	Reserved	
533:532	O	0x0000	Atomic Compare & Write Unit (ACWU)
535:534	M	Reserved	
539:536	O	0x00000000	SGL Support (SGLS)
767:540	Reserved		
1023:768	M	“nqn.2018-05.com.example: nvme:nvm-subststem-OUI00E04C000000”	NVM Subsystem NVMe Qualified Name (SUBNQN)
1791:1024	Reserved		
2047:1792	Refer to the NVMe over Fabrics specification.		
Power State Descriptors			
2079:2048	M	20 03 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 0 Descriptor (PSD0)
2111:2080	O	90 01 00 00 00 00 00 00 00 00 00 00 01 01 01 01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 1 Descriptor (PSD1)
2143:2112	O	2C 01 00 00 00 00 00 00 00 00 00 00 02 02 02 02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 2 Descriptor (PSD2)
2175:2144	O	2C 01 00 03 88 13 00 00 10 27 00 00 03 03 03 03 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 3 Descriptor (PSD3)
2207:2176	O	32 00 00 03 60 EA 00 00 C8 AF 00 00 04 04 04 04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 4 Descriptor (PSD4)
2239:2208	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 5 Descriptor (PSD5)
2271:2240	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 6 Descriptor (PSD6)

		00 00 00 00 00 00 00 00	
2303:2272	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 7 Descriptor (PSD7)
2335:2304	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 8 Descriptor (PSD8)
2367:2336	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 9 Descriptor (PSD9)
2399:2368	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 10 Descriptor (PSD10)
2431:2400	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 11 Descriptor (PSD11)
2463:2432	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 12 Descriptor (PSD12)
2495:2464	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 13 Descriptor (PSD13)
2527:2496	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 14 Descriptor (PSD14)
2559:2528	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 15 Descriptor (PSD15)
2591:2560	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 16 Descriptor (PSD16)

		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	
2623:2592	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 17 Descriptor (PSD17)
2655:2624	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 18 Descriptor (PSD18)
2687:2656	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 19 Descriptor (PSD19)
2719:2688	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 20 Descriptor (PSD20)
2751:2720	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 21 Descriptor (PSD21)
2783:2752	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 22 Descriptor (PSD22)
2815:2784	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 23 Descriptor (PSD23)
2847:2816	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 24 Descriptor (PSD24)
2879:2848	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 25 Descriptor (PSD25)
2911:2880	O	00 00 00 00 00 00 00 00	Power State 26 Descriptor (PSD26)

		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	
2943:2912	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 27 Descriptor (PSD27)
2975:2944	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 28 Descriptor (PSD28)
3007:2976	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 29 Descriptor (PSD29)
3039:3008	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 30 Descriptor (PSD30)
3071:3040	O	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Power State 31 Descriptor (PSD31)
Vendor Specific			
4095:3072	O	52 45 41 4C 54 45 4B 5F 52 4C 36 35 37 37 20 E0 4C 11 6D D6 18 8C 5F 70 5F 74 42 34 37 52 56 05 2E 0C 00 00 00 00 00 00	Vendor Specific (VS)

4.2 SMART/Health Information

Table 4-2 SMART/Health Information log

<table>
<tr><th>Byte</th><th>Description</th></tr>
<tr><td>0</td><td>Critical Warning: This field indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to ‘0’, then that critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the current associated state and are not persistent.
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>00</td><td>If set to ‘1’, then the available spare space has fallen below the threshold.</td></tr>
<tr><td>01</td><td>If set to ‘1’, then a temperature is above an over temperature threshold or below an under temperature threshold (refer to section 5.15.1.4).</td></tr>
<tr><td>02</td><td>If set to ‘1’, then the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability.</td></tr>
<tr><td>03</td><td>If set to ‘1’, then the media has been placed in read only mode.</td></tr>
<tr><td>04</td><td>If set to ‘1’, then the volatile memory backup device has failed. This field is only valid if the controller has a volatile memory backup solution.</td></tr>
<tr><td>07:05</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>2:1</td><td>Composite Temperature: Contains a value corresponding to a temperature in degrees Kelvin that represents the current composite temperature of the controller and namespace(s) associated with that controller. The manner in which this value is computed is implementation specific and may not represent the actual temperature of any physical point in the NVM subsystem. The value of this field may be used to trigger an asynchronous event (refer to section 5.15.1.4).
Warning and critical overheating composite temperature threshold values are reported by the WCTEMP and CCTEMP fields in the Identify Controller data structure in Figure 90.</td></tr>
<tr><td>3</td><td>Available Spare: Contains a normalized percentage (0 to 100%) of the remaining spare capacity available.</td></tr>
<tr><td>4</td><td>Available Spare Threshold: When the Available Spare falls below the threshold indicated in this field, an asynchronous event completion may occur. The value is indicated as a normalized percentage (0 to 100%).</td></tr>
</table>

5	**Percentage Used:** Contains a vendor specific estimate of the percentage of NVM subsystem life used based on the actual usage and the manufacturer's prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed, but may not indicate an NVM subsystem failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state). Refer to the JEDEC JESD218A standard for SSD device life and endurance measurement techniques.
31:6	Reserved
47:32	**Data Units Read:** Contains the number of 512 byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data read to 512 byte units. For the NVM command set, logical blocks read as part of Compare and Read operations shall be included in this value.
63:48	**Data Units Written:** Contains the number of 512 byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data written to 512 byte units. For the NVM command set, logical blocks written as part of Write operations shall be included in this value. Write Uncorrectable commands shall not impact this value.
79:64	**Host Read Commands:** Contains the number of read commands completed by the controller. For the NVM command set, this is the number of Compare and Read commands.
95:80	**Host Write Commands:** Contains the number of write commands completed by the controller. For the NVM command set, this is the number of Write commands.
111:96	**Controller Busy Time:** Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O Queue (specifically, a command was issued via an I/O Submission Queue Tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O Completion Queue). This value is reported in minutes.
127:112	**Power Cycles:** Contains the number of power cycles.
143:128	**Power On Hours:** Contains the number of power-on hours. This may not include time that the controller was powered and in a non-operational power state.

159:144	**Unsafe Shutdowns:** Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
175:160	**Media and Data Integrity Errors:** Contains the number of occurrences where the controller detected an unrecovered data integrity error. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field.
191:176	**Number of Error Information Log Entries:** Contains the number of Error Information log entries over the life of the controller.
195:192	**Warning Composite Temperature Time:** Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater than or equal to the Warning Composite Temperature Threshold (WCTEMP) field and less than the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure in Figure 90. If the value of the WCTEMP or CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
199:196	**Critical Composite Temperature Time:** Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater than the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure in Figure 90. If the value of the CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
201:200	**Temperature Sensor 1:** Contains the current temperature reported by temperature sensor 1. This field is defined by Figure 81.
203:202	**Temperature Sensor 2:** Contains the current temperature reported by temperature sensor 2. This field is defined by Figure 81.
205:204	**Temperature Sensor 3:** Contains the current temperature reported by temperature sensor 3. This field is defined by Figure 81.
207:206	**Temperature Sensor 4:** Contains the current temperature reported by temperature sensor 4. This field is defined by Figure 81.
209:208	**Temperature Sensor 5:** Contains the current temperature reported by temperature sensor 5. This field is defined by Figure 81.
211:210	**Temperature Sensor 6:** Contains the current temperature reported by temperature sensor 6. This field is defined by Figure 81.
213:212	**Temperature Sensor 7:** Contains the current temperature reported by temperature sensor 7. This field is defined by Figure 81.
215:214	**Temperature Sensor 8:** Contains the current temperature reported by temperature sensor 8. This field is defined by Figure 81.
219:216	**Thermal Management Temperature 1 Transition Count**: Contains the number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the

	Composite Temperature because of the host controlled thermal management feature (i.e., the Composite Temperature rose above the Thermal Management Temperature 1.) This counter shall not wrap once it reaches its maximum value. A value of zero, indicates that this transition has never occurred or this field is not implemented.
223:220	**Thermal Management Temperature 2 Transition Count:** Contains the number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance (e.g., heavy throttling) in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature (i.e., the Composite Temperature rose above the Thermal Management Temperature 2.) This counter shall not wrap once it reaches its maximum value. A value of zero, indicates
227:224	**Total Time For Thermal Management Temperature 1:** Contains the number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature. This counter shall not wrap once it reaches its maximum value. A value of zero, indicates that this transition has never occurred or this field is not implemented.
231:228	**Total Time For Thermal Management Temperature 2**: Contains the number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance (e.g., heavy throttling) in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature. This counter shall not wrap once it reaches its maximum value. A value of zero, indicates that this transition has never occurred or this field is not implemented.
511:232	Reserved

4.3 NVMe Command Set

Table 4-3 Admin Command Set

Opcode by Field			Combined Opcode[2]	O/M[1]	Command[3]
(07)	(06:02)	(01:00)			
Standard Command	Function	Data Transfer[4]			
0b	000 00b	00b	00h	M	Delete I/O Submission Queue
0b	000 00b	01b	01h	M	Create I/O Submission Queue
0b	000 00b	10b	02h	M	Get Log Page
0b	000 01b	00b	04h	M	Delete I/O Completion Queue
0b	000 01b	01b	05h	M	Create I/O Completion Queue
0b	000 01b	10b	06h	M	Identify
0b	000 10b	00b	08h	M	Abort
0b	000 10b	01b	09h	M	Set Features
0b	000 10b	10b	0Ah	M	Get Features
0b	000 11b	00b	0Ch	M	Asynchronous Event Request
0b	001 00b	00b	10h	O	Firmware Commit
0b	001 00b	01b	11h	O	Firmware Image Download
0b	001 01b	00b	14h	O	Device Self-test
0b	001 10b	00b	18h	NOTE 5	Keep Alive
1b	000 00b	00b	80h	O	Format NVM
1b	000 00b	01b	81h	O	Security Send
1b	000 00b	10b	82h	O	Security Receive

NOTES:

1. O/M definition: O = Optional, M = Mandatory.
2. Opcodes not listed are reserved.
3. A subset of commands uses the Namespace Identifier field (CDW1.NSID). When not used, the field shall be cleared to 0h.
4. Indicates the data transfer direction of the command. All options to the command shall transfer data as specified or transfer no data. All commands, including vendor specific commands, shall follow this convention: 00b = no data transfer; 01b = host to controller; 10b = controller to host; 11b = bidirectional.
5. For NVMe over PCIe implementations, the Keep Alive command is optional. For NVMe over Fabrics implementations, the associated NVMe Transport binding defines whether the Keep Alive command is optional or mandatory.

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Table 4-4 NVMe Command Set

Opcode by Field			Combined Opcode[2]	O/M[1]	Command[3]
(07)	(06:02)	(01:00)			
Standard Command	Function	Data Transfer[5]			
0b	000 00b	00b	00h	M	Flush
0b	000 00b	01b	01h	M	Write
0b	000 00b	10b	02h	M	Read
0b	000 10b	00b	08h	O	Write Zeroes
0b	000 10b	01b	09h	O	Dataset Management

NOTES:

6. O/M definition: O = Optional, M = Mandatory.
7. Opcodes not listed are reserved.
8. All NVM commands use the Namespace Identifier field (CDW1.NSID).
9. Mandatory if reservations are supported as indicated in the Identify Controller data structure.
10. Indicates the data transfer direction of the command. All options to the command shall transfer data as specified or transfer no data. All commands, including vendor specific commands, shall follow this convention: 00b = no data transfer; 01b = host to controller; 10b = controller to host; 11b = bidirectional.

-Follow NVMe v1.3 Specification

Table 4-5 Log Page Support

Feature Identifier	O/M	Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
05h	O	Commands Supported and Effects
06h	O	Device Self-test

-Follow NVMe v1.3 Specification

Table 4-6 Set Features – Feature Identifiers

Feature Identifier	O/M[6]	Persistent Across Power Cycle and Reset[2]	Uses Memory Buffer for Attributes	Description
00h				Reserved
01h	M	No	No	Arbitration
02h	M	No	No	Power Management
04h	M	No	No	Temperature Threshold
05h	M	No	No	Error Recovery
06h	O	No	No	Volatile Write Cache
07h	M	No	No	Number of Queues
08h	NOTE 5	No	No	Interrupt Coalescing
09h	NOTE 5	No	No	Interrupt Vector Configuration
0Ah	M	No	No	Write Atomicity Normal
0Bh	M	No	No	Asynchronous Event Configuration
0Ch	O	No	Yes	Autonomous Power State Transition
0Dh	O	No[3]	No[4]	Host Memory Buffer
0Fh	O	No	No	Keep Alive Timer
10h	O	Yes	No	Host Controlled Thermal Management
11h	O	No	No	Non-Operational Power State Config

NOTES:

1. The behavior of a controller in response to an inactive namespace ID to a vendor specific Feature Identifier is vendor specific.
2. This column is only valid if the feature is not saveable (refer to section 7.8). If the feature is saveable, then this column is not used and any feature may be configured to be saved across power cycles and reset.
3. The controller does not save settings for the Host Memory Buffer feature across power states and reset events, however, host software may restore the previous values. Refer to section 8.9.
4. The feature does not use a memory buffer for Set Features, but it does use a memory buffer for Get Features. Refer to section 8.9.
5. The feature is mandatory for NVMe over PCIe. This feature is not supported for NVMe over Fabrics.
6. O/M: O = Optional, M = Mandatory.

-Follow NVMe v1.3 Specification

5.0 Pin Assignment and Descriptions

Table 5-1 Pin assignment and descriptions

Top Side			Bottom Side		
NO.	**Pin**	**Descriptions**	**Descriptions**	**Pin**	**NO.**
75	GND	System Ground			
73	GND	System Ground	+3.3V	POWER	74
71	GND	System Ground	+3.3V	POWER	72
69	NC	PDEDC	+3.3V	POWER	70
67	NC	NC	SUSCLK	NC	68
M-KEY					
57	GND	System Ground	NC	NC	58
55	Diff	RefCLKP	NC	NC	56
53	Diff	RefCLKN	PEWAKE#	NC	54
51	GND	System Ground	CLKREQ#	CLKREQ	52
49	Diff	P0RXP	PERST#	PERST	50
47	Diff	P0RXN	NC	NC	48
45	GND	System Ground	NC	NC	46
43	Diff	P0TXP	NC	NC	44
41	Diff	P0TXN	NC	NC	42
39	GND	System Ground	NC	NC	40
37	Diff	P1RXP	NC	NC	38
35	Diff	P1RXN	NC	NC	36
33	GND	System Ground	NC	NC	34
31	Diff	P1TXP	NC	NC	32
29	Diff	P1TXN	NC	NC	30
27	GND	System Ground	NC	NC	28
25	Diff	P2RXP	NC	NC	26
23	Diff	P2RXN	NC	NC	24
21	GND	System Ground	NC	NC	22
19	Diff	P2TXP	NC	NC	20
17	Diff	P2TXN	+3.3V	POWER	18
15	GND	System Ground	+3.3V	POWER	16
13	Diff	P3RXP	+3.3V	POWER	14
11	Diff	P3RXN	+3.3V	POWER	12
9	GND	System Ground	LED1#(OPTION)	LED1#	10
7	Diff	P3TXP	NC	NC	8
5	Diff	P3TXN	NC	NC	6
3	GND	System Ground	+3.3V	POWER	4
1	GND	System Ground	+3.3V	POWER	2

6.0 Product Line up

Table 6-1 Product Line up

Model Name	Capacity	Type	Remark
SM2P32A8-256GC	256GB	M.2 PCIe	0℃~70℃
SM2P32A8-512GC	512GB	M.2 PCIe	
SM2P32A8-001TC	1TB	M.2 PCIe	

Figure 6-1 Model Name Coding Rule

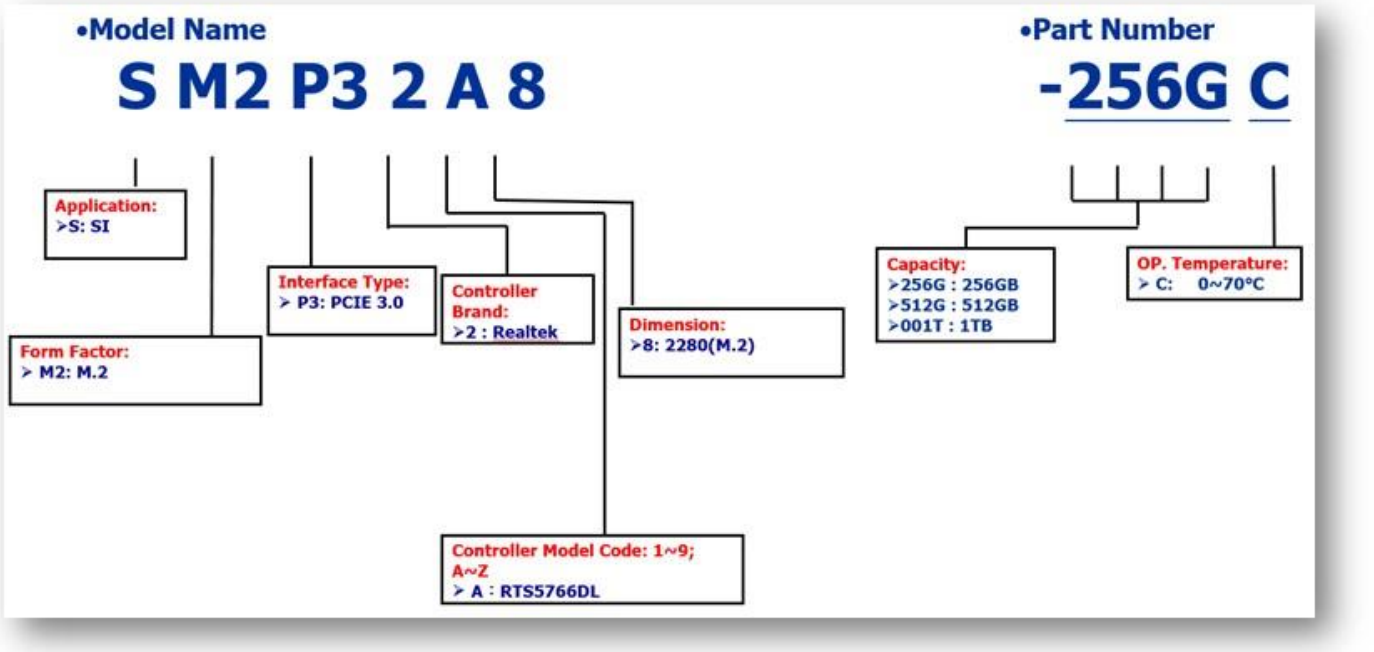

Figure 6-2 Label Pictures

7.0 Package Specification

Figure 7-1 Package Specification